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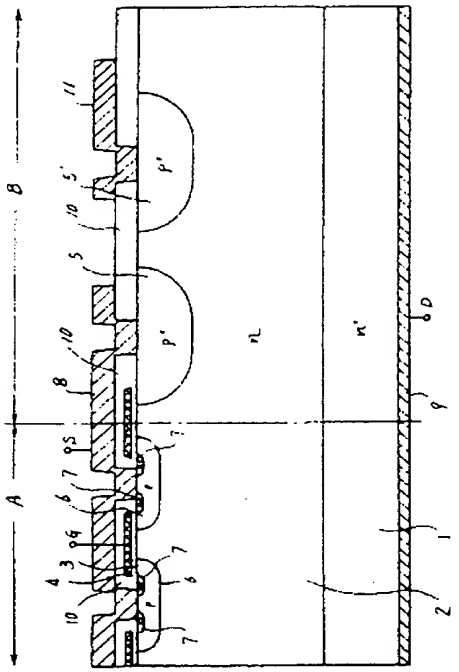
TITLE : INSULATION GATE TRANSISTOR



ABSTRACT : PURPOSE: To obtain the MOST having the characteristics of high withstand voltage and low ON-resistance by a method wherein the depth of the first impurity layer is made larger than that of the second impurity layer by providing the former by surrounding the latter.

CONSTITUTION: A material with an n type low concentration impurity layer 2 formed on an n type Si substrate 1 is used as the semiconductor substrate. In a cell part A, a polycrystalline Si layer is formed on a gate insulation film 3 and then processed into a gate electrode 4, and a base layer 6 is formed by using the electrode 4 as a mask. This base layer 6 is a p type impurity region and is e.g. 10μm deep, whereas a source region 7 formed in the layer 6 is an n type high concentration impurity layer and is e.g. 2μm deep. In the periphery B, p type impurity layers 5 and 5' are e.g. 20μm deep and formed so as to surround the base layer 6 of the cell part A. This construction reduces the dimension of the base layer 6 because the depth of the layer 6 is smaller than the impurity layer 5, resulting in the improvement in current density in the cell part A and to the reduction in ON-resistance.

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